

AUS920040023US1

PATENT

UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	:	Group Art Unit:
Jente B. Kuang et al.	:	Not Yet Assigned
Serial No.: Not Yet Assigned	:	Examiner: Not Yet Assigned
Filed: (herewith)	:	
Title: BUFFER/DRIVER CIRCUITS	:	IBM Corporation
	:	Intellectual Property Law Dept.
	:	11400 Burnet Road
	:	Austin, Texas 78758

INFORMATION DISCLOSURE STATEMENT

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This Information Disclosure Statement is being submitted in connection with the above-identified application for patent. Applicant submits herewith patents, publications or other information of which they are aware, which they believe may be material to the patentability of this application and in respect of which there may be a duty to disclose in accordance with 37 C.F.R. § 1.56.

While this Information Disclosure Statement may be "material" pursuant to 37 C.F.R. § 1.56, it is not intended to constitute an admission that any patent, publication or other information referred to herein is "prior art" for this invention unless specifically designated as such.

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In accordance with 37 C.F.R. § 1.97(g), the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made or that no other material information as defined in 37 C.F.R. § 1.56(a) exists.

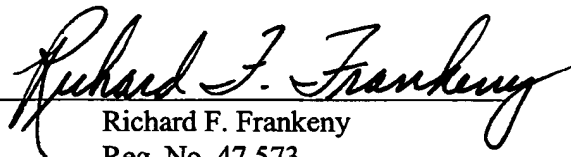
The attached form, PTO-1449, provides a listing of patents, publications, or other information as required by 37 C.F.R. § 1.98(a)(1).

A copy of each of the items identified on the attached Form PTO-1449 is supplied herewith, except for the U.S. patents and the pending patent applications, for which no copies are being submitted.

Respectfully submitted,

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In Place of FORM PTO-1449 (Modified)

LIST OF PATENTS AND PUBLICATIONS FOR APPLICANTS' INFORMATION DISCLOSURE STATEMENT

Serial No.: Not Yet Assigned
 Applicants: Jente B. Kuang et al.
 Filing Date: (herewith)
 Group: Not Yet Assigned
 Atty. Docket No.: AUS920040023US1

Reference Designation

U.S. PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate
____AAA						
____ABA						
____ACA						
____ADA						
____AEA						
____AFA						
____AGA						
____AHA						
____AIA						
____AJA						
____AKA						
____ALA						
____AMA						

FOREIGN PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Country	Class	Subclass	Translation Yes No
____ANA						
____AOA						

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

Examiner Initial

____APA Rafik S. Guindi et al. "Design Techniques for Gate-Leakage Reduction in CMOS in Circuits," *IEEE*, 2003, 5 pages.
 ____AQA
 ____ARA
 ____ASA

Examiner:

Date Considered:

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.